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EXAMINER
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 17

Application Number: 09/503,638
Filing Date: February 14, 2000
Appellant(s): PRALL ET AL.

Steven R. Ormiston
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed May 27, 2003.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 23-25, 28, and 30-33.

Claims 26 and 27 are allowed.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is correct.

(7) *Grouping of Claims*

The rejection of claims 23, 24, 25, 28, 30, 31, 32, and 33 stand or fall together, appellant's brief does include a statement that this grouping of claims does stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) *Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) *Prior Art of Record*

5,444,278	KATAYAMA	8-1995

(10) *Grounds of Rejection*

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 23, 24, 28, and 30-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Katayama.

The structure claimed in claim 23 is anticipated by Katayama, which shows in Fig. 36 a semiconductor memory device that comprises a silicon structure *101* having a first conductivity type; a gate electrode *106* over the silicon structure; a capacitor contact region in the silicon structure *101* adjacent to one side of the gate electrode *106*; a bit line

contact region in the silicon structure *101* adjacent to the other side of the gate electrode *106*; a first dopant implant in the capacitor and bit line contact regions, denoted *103b* and *103a* respectively, the first dopant having a second conductivity type opposite the first conductivity type, as noted in column 19, lines 55-65; and a second dopant implant *104* in only the capacitor contact region.

Regarding claim 24, Katayama shows in Fig. 36, that the second dopant implant *104* is deeper than the first dopant implant *103a* and *103b*.

The structure claimed in claim 28 is anticipated by Katayama, which shows in Fig. 36 a semiconductor memory device that comprises a silicon structure *101* having a first conductivity type; a gate electrode *106* over the silicon structure; a capacitor contact region in the silicon structure *101* adjacent to one side of the gate electrode *106*; a bit line contact region in the silicon structure *101* adjacent to the other side of the gate electrode *106*; a first dopant implant in the capacitor and bit line contact regions, denoted *103b* and *103a* respectively, the first dopant having a second conductivity type opposite the first conductivity type, as noted in column 19, lines 55-65; insulating spacers *107* extending along the sidewalls of the gate electrode and over a portion of the first dopant implant in the capacitor and bit line contact regions; a second dopant implant *104* in only the capacitor contact region, the second dopant implant having the second conductivity type, as shown in column 19, line 55 to column 20, line 3; a capacitor first conductor *112* in electrical contact with the capacitor contact region, the capacitor first conductor comprising silicon doped to the second conductivity type to a level of 10^{20}

atoms per cubic centimeter, as shown in column 20, lines 22-25; a dielectric *113* over the capacitor first conductor *112*; and a capacitor second conductor *114* over the dielectric *113*.

Regarding the feature of the first and second dopant implants being implanted at a dosage of about 10^{13} ions per square centimeter and at an implantation energy in the range of 20 to 100 KeV for the first dopant implant and an implantation energy of up to 200KeV for the second dopant implant it is noted that the method of forming a device is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight. Furthermore, the presence of process limitations on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. *In re Stephens 145 USPQ 656 (CCPA 1965)*.

The structure as claimed in claim 30 is anticipated by Katayama, which shows in Fig. 36 a semiconductor memory device that comprises a substrate *101*; a contact region in the substrate *101*; a first dopant implant *103a, 103b* in the contact region the first implant defining a first implant profile; and a second dopant implant *104* in the contact region, the second implant *104* defining a second implant profile narrower and deeper than the first implant profile.

Regarding claim 31, Katayama discloses that the first and second dopants have the same conductivity type, as shown in col. 19, line 55 to column 20, line 3.

Regarding claim 32, Katayama discloses that the structure further comprises a capacitor in electrical contact with the contact region, as shown in Fig. 36.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama.

The claimed structure is shown by Katayama, which shows in Fig. 36 a semiconductor memory device that comprises a silicon structure *101* having a first conductivity type; a gate electrode *106* over the silicon structure; a capacitor contact region in the silicon structure *101* adjacent to one side of the gate electrode *106*; a bit line contact region in the silicon structure *101* adjacent to the other side of the gate electrode *106*; a first dopant implant in the capacitor and bit line contact regions, denoted *103b* and *103a* respectively, the first dopant having a second conductivity type opposite the first conductivity type, as noted in column 19, lines 55-65; a second dopant implant *104* in only the capacitor contact region; and the second dopant implant *104* is deeper than the first dopant implant *103a* and *103b*.

Katayama teaches all the limitations with the exception of disclosing the depth of the first and second dopant implant.

Katayama teaches energy ranges, and dosage ranges overlapping and included in those taught by the applicant, furthermore the dopant used is the same, as well as the substrate, thus it would have been obvious to one of ordinary skill in the art that the ranges of depth achieved under the same conditions of implantation would be the same or similar and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering optimum or workable ranges involves only routine skill in the art.

(11) Response to Argument

The instant structure essentially comprises a semiconductor memory device that comprises a silicon structure having a first conductivity type; a gate electrode over the silicon structure; a capacitor contact region adjacent to one side of the gate electrode; a bit line contact region adjacent to the other side of the gate electrode; a first dopant implant in both the capacitor and the bit line contact regions; and a second dopant implant in only the capacitor contact region.

Appellant primarily argues that Katayama does not teach two implants at the region contacting the capacitor lower electrode 112, as the capacitor contact region includes implantation layer *104* and then a diffusion layer *105* formed at the region contacting capacitor lower electrode *112*.

It is respectfully submitted that the capacitor contact region, as shown in Fig. 36, comprises the regions *103b*, *104*, and *105*. It is further submitted that regions *103b* and *104* are two implant regions as disclosed in col. 19, line 60, and col. 20, line 3. While it is

correct that the region *105* is a diffusion region, it is respectfully submitted that this region is not relied upon or characterized by the examiner as an implant region, and that the regions relied upon by the examiner are regions *103b*, as the first implant region, and *104*, as the second implant region. It is further submitted that the capacitor contact region is a region where the capacitor makes electrical contact to the gate electrode; therefore region *103b* is part of the capacitor contact region.

Appellant secondarily argues that the examiner has not offered any evidence to support the supposition that a diffusion layer is structurally identical to an implant.

It is respectfully submitted that no evidence is necessary as the examiner relies on two implant regions and the diffusion layer *105* is not relied upon for the teachings of the claims. Furthermore, it is respectfully submitted that the examiner stated that "the presence of process limitations on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product" for the purpose of not giving patentable weight to the limitations of *"the first dopant implanted at a dosage of about 10^{13} ions per square centimeter at an implantation energy in the range of 20 KeV to 100 KeV"* and *"the second dopant implant implanted at a dosage of about 10^{13} ions per square centimeter at an implantation energy up to 200KeV"*, and not to establish that a diffusion region is equivalent to an implant region as the Appellant argues.

In conclusion, it is respectfully submitted that regarding claims 23-24, 28, and 30-32, a prima facie case of anticipation with "specific fact findings for each

contested limitation and satisfactory explanations for such findings" has been presented. *Gechter v. Davidson*, 116 F.3d 1454, 43 USPQ 2s 1030, 1035 (Fed. Cir. 1997). And that a prima facie case of obviousness regarding claims 25 and 33 has been established. While all the evidence of obviousness and non-obviousness has been carefully considered, it is respectfully submitted that the evidence of obviousness would outweigh the evidence of non-obviousness.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Ginette Peralta
August 7, 2003

Appeal Conference held on August 4, 2003.

Conferees:

Olik Chaudhuri OC

Wael Fahmy WF

Ginette Peralta GP